PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ÉTATS-UNIS D'AMÉRIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 28 February 2000 (28.02.00)	
International application No. PCT/BE99/00090	**Applicant's or agent's file reference** P.IMEC.120WO
International filing date (day/month/year) 14 July 1999 (14.07.99)	**Priority date** (day/month/year) 24 July 1998 (24.07.98)
Applicant VAN STEENKISTE, Filip et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

31 January 2000 (31.01.00)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No.: (41-22) 740.14.35

Authorized officer

Olivia RANAIVOJAONA

Telephone No.: (41-22) 338.83.38

WO 00/07229
PCT/BE99/00090

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

To:
VAN MALDEREN, Joëlle
Office Van Malderen
Place Reine Fabiola 6/1
B-1083 Brussels
BELGIQUE

NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION TO THE DESIGNATED OFFICES

(PCT Rule 47.1(c), first sentence)

Date of mailing (day/month/year) 10 February 2000 (10.02.00)	
Applicant's or agent's file reference P.IMEC.120WO	**IMPORTANT NOTICE**

International application No.	**International filing date** (day/month/year)	**Priority date** (day/month/year)
PCT/BE99/00090	14 July 1999 (14.07.99)	24 July 1998 (24.07.98)

Applicant
INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM et al

1. Notice is hereby given that the International Bureau has communicated, as provided in Article 20, the international application to the following designated Offices on the date indicated above as the date of mailing of this Notice:
   AU,CN,EP,IL,JP,KP,KR,US

   In accordance with Rule 47.1(c), third sentence, those Offices will accept the present Notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

2. The following designated Offices have waived the requirement for such a communication at this time:
   AE,AL,AM,AP,AT,AZ,BA,BB,BG,BR,BY,CA,CH,CU,CZ,DE,DK,EA,EE,ES,FI,GB,GD,GE,GH,GM,HR,HU,ID,IN,IS,KE,KG,KZ,LC,LK,LR,LS,LT,LU,LV,MD,MG,MK,MN,MW,MX,NO,NZ,OA,PL,PT,RO,RU,SD,SE,SG,SI,SK,SL,TJ,TM,TR,TT,UA,UG,UZ,VN,YU,ZA,ZW
   The communication will be made to those Offices only upon their request. Furthermore, those Offices do not require the applicant to furnish a copy of the international application (Rule 49.1(a-bis)).

3. Enclosed with this Notice is a copy of the international application as published by the International Bureau on
   10 February 2000 (10.02.00) under No. WO 00/07229

REMINDER REGARDING CHAPTER II (Article 31(2)(a) and Rule 54.2)

If the applicant wishes to postpone entry into the national phase until 30 months (or later in some Offices) from the priority date, **a demand for international preliminary examination** must be filed with the competent International Preliminary Examining Authority before the expiration of 19 months from the priority date.

It is the applicant's sole responsibility to monitor the 19-month time limit.

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

REMINDER REGARDING ENTRY INTO THE NATIONAL PHASE (Article 22 or 39(1))

If the applicant wishes to proceed with the international application in the **national phase**, he must, within 20 months or 30 months, or later in some Offices, perform the acts referred to therein before each designated or elected Office.

For further important information on the time limits and acts to be performed for entering the national phase, see the Annex to Form PCT/IB/301 (Notification of Receipt of Record Copy) and Volume II of the PCT Applicant's Guide.

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer J. Zahra
Facsimile No. (41-22) 740.14.35	Telephone No. (41-22) 338.83.38

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

PCT

To:

VAN MALDEREN, Joelle
Office Van Malderen
Place Reine Fabiola 6/1
B-1083 Brussels
BELGIQUE

NOTIFICATION OF RECEIPT OF DEMAND BY COMPETENT INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

(PCT Rules 59.3(e) and 61.1(b), first sentence and Administrative Instructions, Section 601(a))

Date of mailing *(day/month/year)*	23.02.00
Applicant's or agent's file reference: P.IMEC.120WO	IMPORTANT NOTIFICATION

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/BE 99/00090	14/07/1999	24/07/1998

Applicant

INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM et al.

1. The applicant is hereby **notified** that this International Preliminary Examining Authority considers the following date as the date of receipt of the demand for international preliminary examination of the international application:

31/01/2000

2. This date of receipt is:

☒ the actual date of receipt of the demand by this Authority (Rule 61.1(b)).

☐ the actual date of receipt of the demand on behalf of this Authority (Rule 59.3(e)).

☐ the date on which this Authority has, in response to the invitation to correct defects in the demand (Form PCT/IPEA/404), received the required corrections.

3. ☐ **ATTENTION:** That date of receipt is **AFTER** the expiration of 19 months from the priority date. Consequently, the election(s) made in the demand does (do) not have the effect of postponing the entry into the national phase until 30 months from the priority date (or later in some Offices) (Article 39(1)). Therefore, the acts for entry into the national phase must be performed within 20 months from the priority date (or later in some Offices) (Article 22). For details, see the *PCT Applicant's Guide*, Volume II.

☐ *(If applicable)* This notification confirms the information given by telephone, facsimile transmission or in person on:

4. Only where paragraph 3 applies, a copy of this notification has been sent to the International Bureau.

Name and mailing address of the IPEA/	Authorized officer
European Patent Office D-80298 Munich Tel. (+49-89) 2399-0, Tx: 523656 epmu d Fax: (+49-89) 2399-4465	NOVELLI C Tel. (+49-89) 2399-8641

OFFICE EUROPÉEN DES BREVETS · EUROPÄISCHES PATENTAMT · EUROPEAN PATENT OFFICE

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
P.IMEC.120WO		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/BE 99/ 00090	14/07/1999	24/07/1998

Applicant

INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM et al.

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 2

   [X] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/BE 99/00090

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/288 H01L23/48 H01L23/482 H01L23/485

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 009, no. 288 (E-358), 15 November 1985 (1985-11-15) & JP 60 128615 A (SUMITOMO DENKI KOGYO KK), 9 July 1985 (1985-07-09) abstract ---	1,5,9
X	US 4 939 568 A (TAGUCHI MASAO ET AL) 3 July 1990 (1990-07-03) column 4, line 46 -column 6, line 4 figure 4G ---	8
A	PATENT ABSTRACTS OF JAPAN vol. 006, no. 254 (E-148), 14 December 1982 (1982-12-14) & JP 57 153431 A (MITSUBISHI DENKI KK), 22 September 1982 (1982-09-22) abstract --- -/--	1,5,9

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 October 1999	12/10/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	van der Linden, J

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/BE 99/00090

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 780 890 A (COMMISSARIAT ENERGIE ATOMIQUE) 25 June 1997 (1997-06-25) column 5, line 41 -column 6, line 43 figure 4	2,3
A	FR 1 555 930 A (PHILIPS GLOEILAMPFABRIEK) 31 January 1969 (1969-01-31) page 2, left-hand column, paragraph 4 -page 2, right-hand column, paragraph 1 figure 4	4,13
A	DE 28 30 761 A (BOSCH GMBH ROBERT) 24 January 1980 (1980-01-24) claims 1-4	6,7,14

1

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/BE 99/00090

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 60128615 A	09-07-1985	NONE	
US 4939568 A	03-07-1990	JP 1709516 C	11-11-1992
		JP 3074508 B	27-11-1991
		JP 62219954 A	28-09-1987
		JP 62272556 A	26-11-1987
		DE 3778944 A	17-06-1992
		EP 0238089 A	23-09-1987
JP 57153431 A	22-09-1982	NONE	
EP 0780890 A	25-06-1997	FR 2742452 A	20-06-1997
		JP 9195094 A	29-07-1997
		US 5828133 A	27-10-1998
FR 1555930 A	31-01-1969	NL 6701136 A	26-07-1968
		BE 709772 A	23-07-1968
		CH 479162 A	30-09-1969
		DE 1614306 A	20-08-1970
		ES 349652 A	01-04-1969
		GB 1204263 A	03-09-1970
		SE 350648 B	30-10-1972
		US 3528090 A	08-09-1970
DE 2830761 A	24-01-1980	NONE	

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
P.IMEC.120WO		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/BE99/00090	14/07/1999	24/07/1998
International Patent Classification (IPC) or national classification and IPC H01L21/288		
Applicant INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 2 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
31/01/2000	17.10.2000
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Krause, J Telephone No. +49 89 2399 2829

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/BE99/00090

I. Basis of the report

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

Description, pages:

1-11	as originally filed				

Claims, No.:

1-6	as received on	31/08/2000	with letter of	28/08/2000	

Drawings, sheets:

1/3-3/3	as originally filed

2. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

V. Reasoned statem nt under Article 35(2) with regard to novelty, inv ntive step or industrial applicability; citations and explanati ns supporting such statem nt

1. Statement

Novelty (N)	Yes:	Claims 1 - 6
	No:	Claims
Inventive step (IS)	Yes:	Claims 1 - 6
	No:	Claims
Industrial applicability (IA)	Yes:	Claims 1 - 6
	No:	Claims

2. Citations and explanations

see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Concerning Section V:

I. Claim 1:

1. The document Patent Abstracts of Japan, vol. 6, No. 254 (E-148);& JP-A-57 153 431 (= D1) describes a method for plating on at least one conductive pattern on a surface of a substrate (1), said substrate having at least a first surface (2) and a second surface, said method comprising the steps of placing the substrate on an electrode (7) being part of a plating holder (6, 9) such that said second surface of said substrate is in contact with said electrode and said conductive pattern is temporarily electrically connected to said electrode via the substrate (the conductive pattern is of course also connected to itself), and applying a plating solution on said first surface of said substrate, thereby inhibiting exposure of said second surface to said plating solution.

2. According to the characterising part of claim 1 a contact is provided on the first surface of the substrate, which is connected to the electrode and to the conductive pattern to be plated. As has been set out in the description of the present application (cf. page 2, lines 2 to 10), a contact may be formed in the peripheral region of a wafer and be in contact with the electrode. However, in this case a contact of the electrode with the lower surface is not described. A connection of the contact with the conductive pattern by a polysilicon conductor is a routine option for the skilled person but not mentioned in document D1.

3. The document US-A-4 939 568 (= D2) describes a three-dimensional integrated circuit structure (cf. column 4, line 46, to column 6, line 21, column 6, line 58, to column 7, line 2, and Figs 4(a) to 4(j)), in which a metal pattern (106) is connected to the substrate via a polysilicon layer (27, 28). In document D2 the polysilicon layer is connected to the lower substrate surface via contacts (6b). However, the person skilled in the art is not led to place the substrate of document D2 onto a plating electrode.

4. As a consequence, the subject-matter of claim 1 would not be readily obtainable by the person skilled in the art, and therefore claim 1 is considered to meet the

requirements of Article 33(2) and (3) PCT.

5. Claims 2 to 5 depend on claim 1, ie they comprise all the features of claim 1. Since claims 1 is considered to meet the requirements of Article 33(2) and (3) PCT, also claims 2 to 5 appear to meet these requirements.

II. Claim 6:

1. Document D2 describes a substrate (1) having at least a first surface and a second surface opposite to said first surface (cf. in particular Figs 4(h), 4(j), and the associated text), said first surface being exposable to a plating solution, said substrate comprising a conductive pattern (6b) being positioned at said first surface of the substrate, a contact (4a, 4b) to the first surface of the substrate, and said conductive pattern being temporarily electrically connected by a polysilicon conductor (27, 28) with said contact (6b) and said contact being electrically connected with said second surface.

2. The subject-matter of claim 6 differs therefrom only by the support plate (36) which is fixed on the first surface of the substrate. This support plate is removed later on. The argument of the applicants put forward in their letter of 28 August 2000 is not convincing in this respect, cf. in D2 column 7, lines 49 to 59. However, before the support plate is removed, a second IC substrate is stacked on the second surface, so that both surfaces are not free at the same time.

3. In the course of the process described in D2 no substrate is obtained which comprises all the features of claim 6, and the applicants are correct in stating that there is no incentive in D2 to vary the process such that a substrate with two connected surfaces is obtained. For the process of D2 such a variation would not result in an advantage, and therefore the arguments of the applicants in their letter of 28 August 2000 are accepted in this respect.

4. As a consequence, the substrate according to claim 6 would not be obtained by a routine variation of the process described in document D2, and therefore claim 6 is considered to meet the requirements of Article 33(2) and (3) PCT.

Concerning Section VII:

1. Independent claims 6 is not in the two-part form in accordance with Rule 6.3(b) PCT, which in the present case would be appropriate, with those features known in combination from the prior art (cf. document D2) being placed in the preamble (Rule 6.3(b)(i) PCT) and with the remaining features being included in the characterising part (Rule 6.3(b)(ii) PCT).

2. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1 and D2 are not mentioned in the description, nor are these documents identified therein.

Concerning Section VIII:

1. In claim 6 it is specified that the conductive pattern should be temporarily connected to the contact. Since claim 6 is directed to a device, the word "temporarily" does not make sense. The device according to claim 6 should be protected when the connection is present (Article 6 PCT).

CLAIMS

1. A system for plating on at least one conductive pattern, said conductive pattern being positioned at a first surface of a substrate having at least a first surface and a second surface, said system comprising:

a support with an electrically connectable electrode thereon;

a sealing element to inhibit the exposure of the second surface of the substrate to a plating solution; and

where said substrate is placeable on said support such that said electrode is in contact with said second surface of said substrate and wherein a contact to said first surface of said substrate is provided, said conductive pattern being temporary electrically connected with said contact and said contact being electrically connected with said electrode.

2. The system as recited in claim 1, wherein said conductive pattern is temporary electrically connected with said contact to the first surface of the substrate by a polysilicon conductor or an amorphous silicon conductor.

3. The system as recited in claim 2, where said conductive pattern is positioned on a first die and said contact is positioned on a second die different from said first die.

4. The system as recited in claim 1, where a part of said conductive pattern at said first surface is covered with a resist layer to inhibit plating on said part.

5. The system as recited in claim 1, where said substrate is a piece of a conductive material or a doped semi-conductive material.

6. The system as recited in claim 1, where said second surface of a substrate is provided with a metal contact.

7. A system as recited in claim 1, where said plating solution comprises an element selected from a group comprising Ag, Cu, Au, Pt, Ti, Ni and Co.

8. A substrate having at least a first surface and a second surface opposite to said first surface, said first surface being exposable to a plating solution, said substrate comprising

a conductive pattern being positioned at said first surface of a substrate;

a contact to the first surface of the substrate; and

said conductive pattern being temporary electrically connected by a polysilicon or an amorphous silicon conductor with said contact and said contact being electrically connected with said second surface.

9. A method for plating on at least one conductive pattern on a surface of a substrate, said substrate having at least a first surface and a second surface, said method comprising the steps of:

placing the substrate on an electrode being part of a plating holder such that said second surface of said substrate is in contact with said electrode and said conductive pattern is temporary electrically connected to said conductive pattern; and

applying a plating solution on said first surface of said substrate thereby inhibiting exposure of said second surface to said plating solution.

10. A method as recited in claim 9, wherein said electrode and said conductive pattern are temporary electrically connected by forming a polysilicon or an amorphous silicon conductor to temporary connect said

conductive pattern with a contact to the substrate, said contact being formed on the first surface of the substrate, and by providing an electrical connection between said contact and said electrode.

11. A method as recited in claim 10, wherein said conductive pattern is positioned on a first die and said contact is positioned on a second die different from said first die.

12. A method as recited in claim 11, wherein after said conductive pattern is plated, said method further comprises the step of dicing the substrate

13. A method as in claim 9, wherein prior to applying the plating solution, a resist layer is deposited on said conductive pattern and patterned in order to create at least one covered area an at least one uncovered area, said uncovered area being exposable to said plating solution.

14. A method as recited in claim 9, where said plating solution comprises an element selected from a group comprising Ag, Cu, Au, Pt, Ti, Ni and Co.

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H01L 21/288, 23/48, 23/482, 23/485 — A1

(11) International Publication Number: **WO 00/07229**

(43) International Publication Date: 10 February 2000 (10.02.00)

(21) International Application Number: PCT/BE99/00090

(22) International Filing Date: 14 July 1999 (14.07.99)

(30) Priority Data:
06/093,974 24 July 1998 (24.07.98) US

(71) Applicants *(for all designated States except US)*: INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM [BE/BE]; Vereniging Zonder Winstbejag, Kapeldreef 75, B-3001 Heverlee (BE). SIEMENS AKTIENGESELLSCHAFT [DE/DE]; Wittelsbacherplatz 2, D-80333 München (DE).

(72) Inventors; and

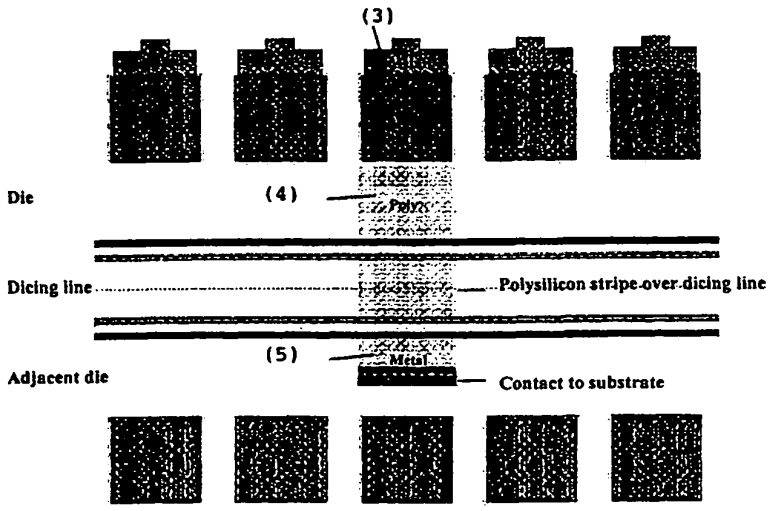
(75) Inventors/Applicants *(for US only)*: VAN STEENKISTE, Filip [BE/BE]; Hoevestraat 12, B-9870 Machelen (BE). BAERT, Kris [BE/BE]; St. Jorislaan 9, B-3001 Leuven (BE). GUMBRECHT, Walter [DE/DE]; In der Rote 1, D-91074 Herzogenaurach (DE). ARQUINT, Philippe [DE/DE]; Stegerstrasse 13A, D-91074 Herzogenaurach (DE).

(74) Agents: VAN MALDEREN, Joëlle et al.; Office Van Malderen, Place Reine Fabiola 6/1, B-1083 Brussels (BE).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: A SYSTEM AND A METHOD FOR PLATING OF A CONDUCTIVE PATTERN



(57) Abstract

The invention presents methods and systems for plating conductive patterns which at least result in a high uniformity and avoid parasitical plating effects. A plating system is disclosed for plating conductive patterns formed at a first surface of a substrate. The system is such that exposure to surfaces not to be plated is inhibited. A first electrode of the system is immersed in the plating solution while the second electrode is in contact with another than said first surface of the substrate. The conductive patterns to be plated are temporarily electrically connected with the second electrode.

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A SYSTEM AND A METHOD FOR PLATING OF A CONDUCTIVE PATTERN

Field of the invention

The invention relates to methods and systems for plating conductive patterns.

Technological background

In the solid state electronics industry, a plurality of components being active devices as well as passive devices are processed on a surface of a semiconductor wafer for instance to form an integrated circuit. To form these integrated circuits metallization structures are requested both as a part of the aforementioned devices and to interconnect these devices. The formation of such metallization structures includes the plating of a conductive pattern, being part of a metallization structure and being formed at a first surface of a substrate, such as a wafer. Particularly this first surface can be the front side or the back side of the wafer.

One of the issues involved is the plating of this first surface of a substrate without exposing a second surface of a wafer, opposite to the first surface, to a plating solution. Particularly, exposure, even partly, would result in unwanted wetting, plating and/or corroding of other surfaces. Furthermore to be able to deposit a material by electroplating, the plating solution must be in contact with the first surface of the substrate comprising

the conductive patterns to be plated and two electrically connectable electrodes have to be provided. Usually, the first electrode is immersed in the plating solution, while the second electrode has to be electrically connected to the conductive patterns to be plated. State-of-the-art plating techniques usually contact peripheral regions of the first surface of a substrate, comprising the conductive patterns to be plated. These peripheral contact regions are electrically connected to the second electrode as well as to the conductive patterns to be plated.

A problem is that often long metal lines are required to connect each conductive pattern to be plated with the contact in the peripheral region. Particularly, this is a problem when one wants to perform plating on wafer scale because the differences in distance between conductive patterns to be plated being located near the edges of the wafer and in the center of the wafer are huge. These differences are typically in the centimeter range. Consequently also the differences in resistance of the metal lines connecting the respective conductive patterns can be huge. This often results in a highly non-uniform plating process. All these metal connections between the conductive patterns to be plated and the peripheral regions can not be easily removed after the plating process and moreover, a lot of wafer-area is required to provide these connections thereby inhibiting dense integration. Another problem is that the contact means in the peripheral regions are exposed to the plating solution. These contact means become parasitically plated and have to be cleaned regularly. A further problem can arise if the contact means do not simultaneously can be used as sealing means, then extra sealing means are required. These sealing means should then be positioned between the contact means and the edges of the wafer in order to avoid leakage of the plating

solution to another surface of the wafer. Consequently, this leads again to a further decrease of the available area which can be plated.

Aim of the invention

The invention presents methods and systems for plating conductive patterns which at least result in a high uniformity and avoid parasitical plating effects.

Summary of the invention

In an aspect of the invention a plating system is disclosed for plating on a plurality of conductive patterns formed at a surface of a substrate. A plating solution is applied on this surface and the exposure of other surfaces of the substrate to the plating solution is inhibited. A first electrode of the system is immersed in the plating solution while the second electrode is in contact with another surface of the substrate. The conductive patterns to be plated are temporary electrically connected with the second electrode resulting in a uniform and selective deposition over the exposed surface of the substrate. Particularly, according to this aspect of the invention, a system is disclosed for plating on at least one conductive pattern, said conductive pattern being positioned at a first surface of a substrate having at least a first surface and a second surface, said system comprising:

a support with an electrically connectable electrode thereon;

a sealing element to inhibit the exposure of the second surface of the substrate to a plating solution; and

wherein said substrate is placeable on said support such that said electrode is in contact with said

second surface of said substrate and wherein a contact to said first surface of said substrate is provided, said conductive pattern being temporary electrically connected with said contact and said contact being electrically connected with said electrode.

In another aspect of the invention, a substrate is disclosed having at least a first surface and a second surface opposite to said first surface, said first surface being exposable to a plating solution, said substrate comprising

a conductive pattern being positioned at said first surface of a substrate;

a contact to the first surface of the substrate; and

said conductive pattern being temporary electrically connected by a polysilicon or an amorphous silicon conductor with said contact and said contact being electrically connected with said second surface.

In a further aspect of the invention, a method is disclosed for plating on at least one conductive pattern formed at a surface of a substrate, said substrate having at least a first surface and a second surface, said method comprising the steps of:

placing the substrate on an electrode being part of a plating holder such that said second surface of said substrate is in contact with said electrode and said conductive pattern is temporary electrically connected to said conductive pattern; and

applying a plating solution on said first surface of said substrate thereby inhibiting exposure of said second surface to said plating solution.

Brief description of the drawings

Figure 1 shows a plurality of structures to be plated. Each one of said plurality of structures (with boundary (2)) is connected to a polysilicon stripe which crosses the dicing line (1).

Figure 2 shows a metal (3) of a first die and a second die, being adjacent. The polysilicon stripe (4) extends from said metal (3) over the dicing line (1) and is further connected to the substrate contact (5) on said second die.

Figure 3 shows a system for plating, comprising of a plating holder with a backside contact. Means for sealing (6), preventing the second surface of the wafer being exposed to the plating solution are foreseen. A backside contact means is also present.

Figure 4 shows a cross-section view of the polysilicon stripes. Dicing over the polysilicon stripe, results in disconnecting the electroplated structures from the substrate contact.

Figure 5 shows a top vies of the polysilicon stripes.

Description of the invention

In an aspect of the invention a plating system is disclosed for plating on a plurality of conductive patterns formed at a surface of a substrate. A plating solution is applied on this surface and the exposure of other surfaces of the substrate to the plating solution is inhibited. A first electrode of the system is immersed in the plating solution while the second electrode is in contact with another surface of the substrate. The conductive patterns to be plated are temporary electrically connected with the second electrode resulting in a uniform and selective deposition over the exposed surface of the

substrate. Particularly, according to this aspect of the invention, a system is disclosed for plating on at least one conductive pattern, said conductive pattern being positioned at a first surface of a substrate having at least a first surface and a second surface, said system comprising:

a support with an electrically connectable electrode thereon;

a sealing element to inhibit the exposure of the second surface of the substrate to a plating solution; and

where said substrate is placeable on said support such that said electrode is in contact with said second surface of said substrate and wherein a contact to said first surface of said substrate is provided, said conductive pattern being temporary electrically connected with said contact and said contact being electrically connected with said electrode. Particularly, the electrical connection between the contact at the first surface of the substrate and the electrode at the second surface of the substrate can be a doped semi-conductive region of either an n-type conductivity or a p-type conductivity, or a metal via connection extending from the first surface to the second surface of the substrate. Furthermore, a metal contact can be provided at the second surface of the substrate.

In an embodiment of the invention a system is disclosed for plating on a plurality of conductive patterns formed at a surface of a substrate. Each conductive pattern to be plated is temporary electrically connected with a contact to the first surface of the substrate by a polysilicon conductor or an amorphous silicon conductor. Particularly, the conductive pattern is positioned on a first die and the corresponding contact is positioned on a

second die different from said first die. Preferably said second die is adjacent to said first die to keep the polysilicon or amorphous silicon conductor as short as possible to minimize the resistance of the connection. Consequently the plating can be performed in a substantially uniform manner.

In another embodiment of the invention a system is disclosed for plating on a plurality of conductive patterns formed at a surface of a substrate, where at least a part of a conductive pattern and/or a contact to a first surface of a substrate is covered with a layer to inhibit plating on said part. Particularly this layer can be a resist layer. By doing so the usually undesired plating of a contact to the first surface of the substrate can be avoided.

The substrate can be a piece of a conductive material or a doped semi-conductive material. Particularly a silicon semiconductor wafer of a n-type or p-type conductivity can be used. The plating solution can be any commercially available plating solution. Of particular interest are plating solutions containing an element selected from a group comprising Ag, Cu, Au, Pt, Ti, Ni and Co. The conductive patterns are usually metal patterns. Particularly Al-containing or Cu-containing patterns can be used.

In another aspect of the invention, a substrate is disclosed having at least a first surface and a second surface opposite to said first surface, said first surface being exposable to a plating solution, said substrate comprising

a conductive pattern being positioned at said first surface of a substrate;

a contact to the first surface of the substrate; and

said conductive pattern being temporary electrically connected by a polysilicon or an amorphous silicon conductor with said contact and said contact being electrically connected with said second surface.

In a further aspect of the invention, a method is disclosed for plating on at least one conductive pattern formed at a surface of a substrate, said substrate having at least a first surface and a second surface, said method comprising the steps of:

placing the substrate on an electrode being part of a plating holder such that said second surface of said substrate is in contact with said electrode and said conductive pattern is temporary electrically connected to said conductive pattern; and

applying a plating solution on said first surface of said substrate thereby inhibiting exposure of said second surface to said plating solution.

In another embodiment of the invention, a plating solution is disclosed wherein said electrode and said conductive pattern are temporary electrically connected by forming a polysilicon or an amorphous silicon conductor to temporary connect said conductive pattern with a contact to the substrate, said contact being formed on the first surface of the substrate, and by providing an electrical connection between said contact and said electrode. The resistance of the electrical connection between the contact and the electrode is substantially independent of the location of the contact on the first surface of the substrate. Therefore, to achieve a high degree of uniformity over the substrate of the plating process, preferably the length of the polysilicon or the amorphous silicon conductor should be kept as short as possible. On the other hand, one has to be able to easily cut the connection provided by the silicon or the amorphous

silicon conductor after the plating process. Therefore, preferably, the conductive pattern is positioned on a first die and said contact is positioned on a second die different from said first die. By doing so, the connection can by cut by dicing the substrate. More preferably, said first and said second die are adjacent dies.

In another embodiment of the invention a method is disclosed, wherein prior to applying the plating solution, a resist layer is deposited on said conductive pattern and patterned in order to create at least one covered area an at least one uncovered area, said uncovered area being exposable to said plating solution.

In an embodiment of the invention, as an example, a system and a method for selectively electroplating a plurality of aluminum patterns is disclosed. The aluminum patterns to be plated are formed on the front side of a silicon wafer with a p-type conductivity. Each aluminum pattern (Fig. 1) to be plated is connected by means of a polysilicon line to an aluminum contact to the p-type substrate region of the wafer at the front side of the wafer. This contact is positioned on an adjacent die. The polysilicon line is isolated from the wafer by means of at least one dielectric layer. The polysilicon line extends over a dicing line (Fig. 2). Accordingly, all aluminum patterns to be plated are electrically connected to the back side of the wafer which can be provided with an aluminum metal contact.

Before applying a plating solution, the wafer is placed on a support with an electrically connectable electrode thereon such that there is an electrical connection between the back side of the wafer and the electrode. This support is a part of a wafer holder designed for plating purposes. During the plating process, the plating solution is brought in contact with the front

side of the wafer, while the backside is sealed by means of a sealing element being part of the aforementioned wafer holder (Fig. 3). Particularly, this sealing element is a sealing ring which inhibits the exposure of the backside of the substrate to the plating solution The backside of the wafer is electrically connected with a backside electrode of the same size. By immersing a similar electrode as counter electrode in the plating solution, a homogeneous electrical field can be created. The plating process is galvanostatic, e.g. the current is held constant by regulating the potential between the backside and the counter electrode. According to the example, silver is electroplated and an alkaline silver solution is used as plating solution. A negative potential is applied at the backside electrode.

In order to avoid plating of the aluminium contacts to the substrate at the front side of the substrate, a positive photoresist layer (AZ4562) is used to cover those areas where no plating may occur.

Finally, the wafers are stripped and diced. Figure 4 and figure 5 show respectively a cross-section and top view of the polysilicon lines. By dicing over the polysilicon lines, the electroplated structures are disconnected from the respective substrate contact.

By using the substrate as a contacting layer for an electrode, the electrical resistance between the areas to be plated and the electrical contact point is for all plated structures substantially the same, particularly if the length of the polysilicon lines is kept sufficiently short and the specific resistance of the polysilicon line is sufficiently low. This length has to be sufficiently short to assure that the resistance of the polysilicon lines has a negligible contribution to the total resistance of the connection between the conductive pattern and the

backside of the wafer. Accordingly, the uniformity of the plating process is increased or in another words, the homogeneity of the deposited thickness of the plated material over the complete wafer is increased. In the example, the plated material is silver.

By dicing over the polysilicon lines, the individual electroplated patterns are disconnected one from the other and are no longer in contact with the substrate. By using polysilicon or amorphous silicon lines extending over the dicing lines, the risk to create electroplated patterns, being short-circuited to the substrate after dicing is reduced. If metal lines or leads would be used to provide the connection to the contact extending over the dicing line, the electroplated patterns can still be in contact with the substrate after dicing due to metal shavings or residues.

The same plating system and method as defined according the present invention can be used for electrochemical chloridation on wafer scale provided that a different solution is used and a positive potential is applied at the backside electrode instead of a negative potential. Of particular interest is the electrochemical chloridation of silver. The electrochemical chloridation of bulk silver electrodes (wires) can be used for producing standard reference electrodes. An advantage is that the quality of the AgCl layer formed by using electrochemical chloridation is better than by using a chemical chloridation. So, according to the present invention, Ag/AgCl reference electrodes on wafer scale can be formed by using electroplated silver and electrochemically chloridized silver chloride.

CLAIMS

1. A system for plating on at least one conductive pattern, said conductive pattern being positioned at a first surface of a substrate having at least a first surface and a second surface, said system comprising:

a support with an electrically connectable electrode thereon;

a sealing element to inhibit the exposure of the second surface of the substrate to a plating solution; and

where said substrate is placeable on said support such that said electrode is in contact with said second surface of said substrate and wherein a contact to said first surface of said substrate is provided, said conductive pattern being temporary electrically connected with said contact and said contact being electrically connected with said electrode.

2. The system as recited in claim 1, wherein said conductive pattern is temporary electrically connected with said contact to the first surface of the substrate by a polysilicon conductor or an amorphous silicon conductor.

3. The system as recited in claim 2, where said conductive pattern is positioned on a first die and said contact is positioned on a second die different from said first die.

4. The system as recited in claim 1, where a part of said conductive pattern at said first surface is covered with a resist layer to inhibit plating on said part.

5. The system as recited in claim 1, where said substrate is a piece of a conductive material or a doped semi-conductive material.

6. The system as recited in claim 1, where said second surface of a substrate is provided with a metal contact.

7. A system as recited in claim 1, where said plating solution comprises an element selected from a group comprising Ag, Cu, Au, Pt, Ti, Ni and Co.

8. A substrate having at least a first surface and a second surface opposite to said first surface, said first surface being exposable to a plating solution, said substrate comprising

a conductive pattern being positioned at said first surface of a substrate;

a contact to the first surface of the substrate; and

said conductive pattern being temporary electrically connected by a polysilicon or an amorphous silicon conductor with said contact and said contact being electrically connected with said second surface.

9. A method for plating on at least one conductive pattern on a surface of a substrate, said substrate having at least a first surface and a second surface, said method comprising the steps of:

placing the substrate on an electrode being part of a plating holder such that said second surface of said substrate is in contact with said electrode and said conductive pattern is temporary electrically connected to said conductive pattern; and

applying a plating solution on said first surface of said substrate thereby inhibiting exposure of said second surface to said plating solution.

10. A method as recited in claim 9, wherein said electrode and said conductive pattern are temporary electrically connected by forming a polysilicon or an amorphous silicon conductor to temporary connect said

conductive pattern with a contact to the substrate, said contact being formed on the first surface of the substrate, and by providing an electrical connection between said contact and said electrode.

11. A method as recited in claim 10, wherein said conductive pattern is positioned on a first die and said contact is positioned on a second die different from said first die.

12. A method as recited in claim 11, wherein after said conductive pattern is plated, said method further comprises the step of dicing the substrate

13. A method as in claim 9, wherein prior to applying the plating solution, a resist layer is deposited on said conductive pattern and patterned in order to create at least one covered area an at least one uncovered area, said uncovered area being exposable to said plating solution.

14. A method as recited in claim 9, where said plating solution comprises an element selected from a group comprising Ag, Cu, Au, Pt, Ti, Ni and Co.

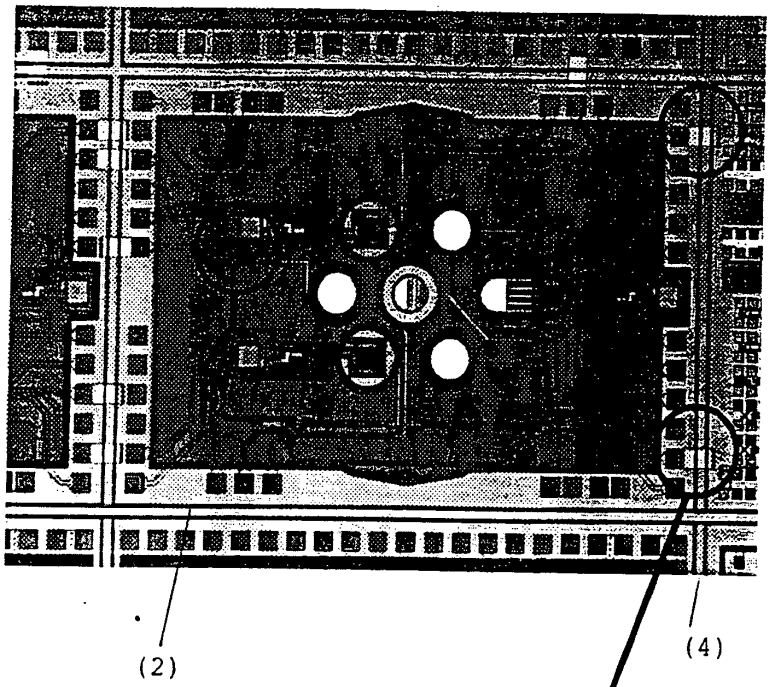
(2)
(4)

FIG. 1

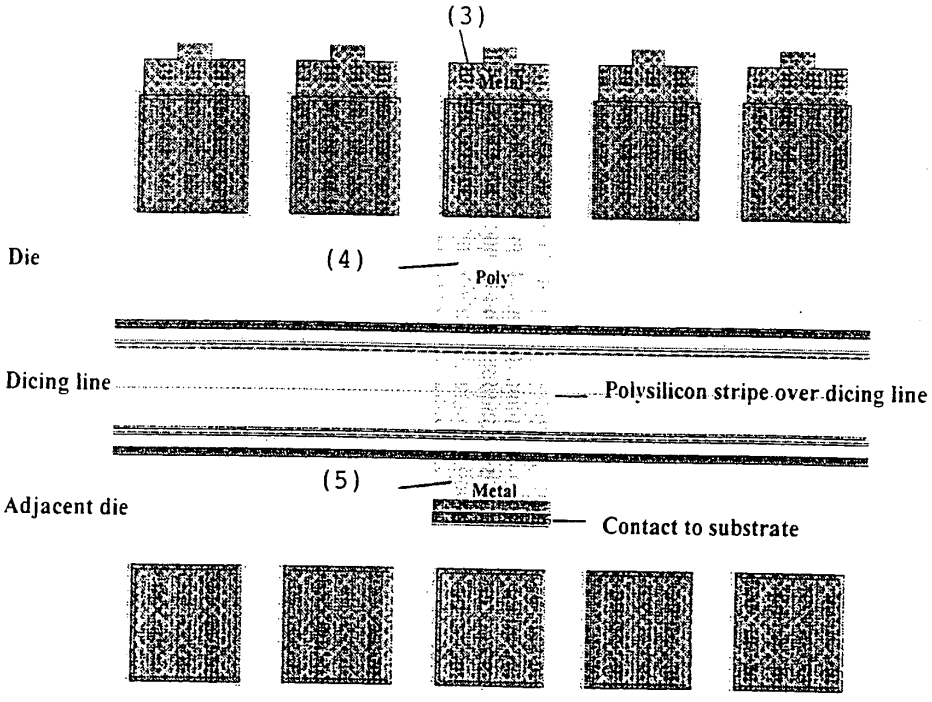
(3)
Metal
Die
(4)
Poly
Dicing line
Polysilicon stripe over dicing line
(5)
Metal
Adjacent die
Contact to substrate

FIG. 2

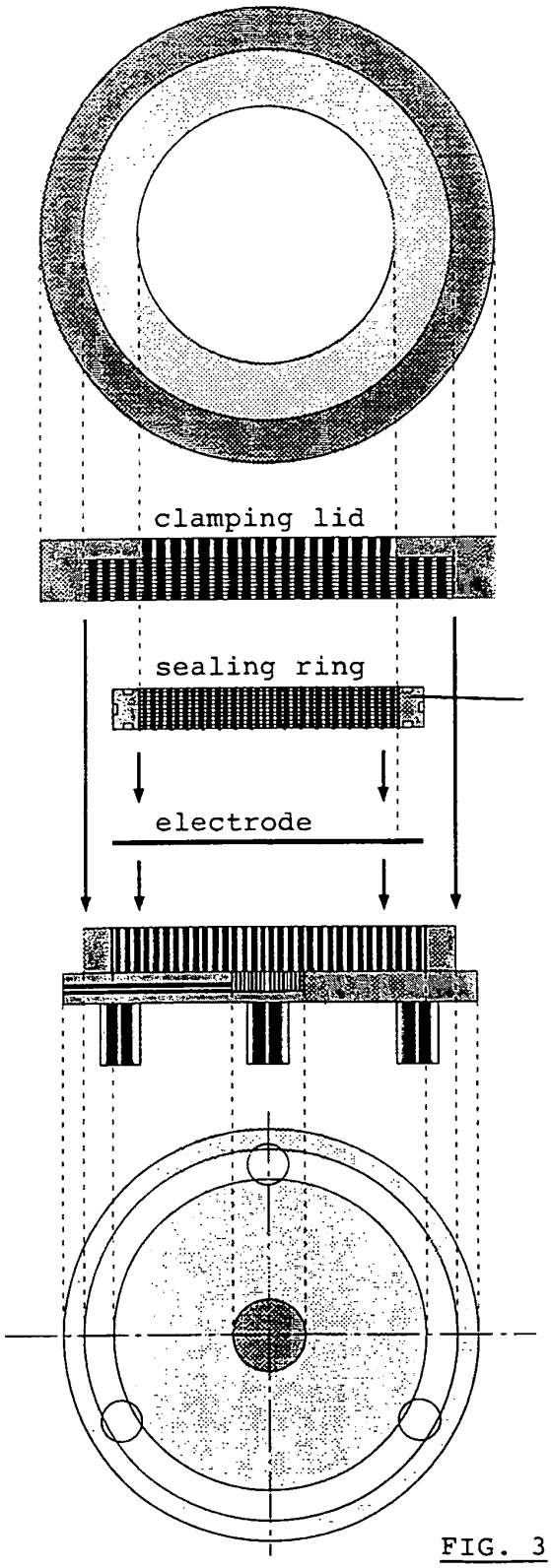

FIG. 3

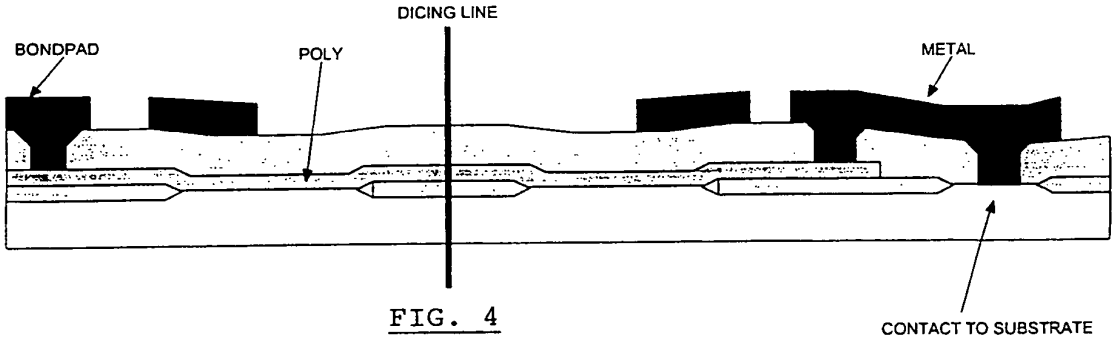

FIG. 4

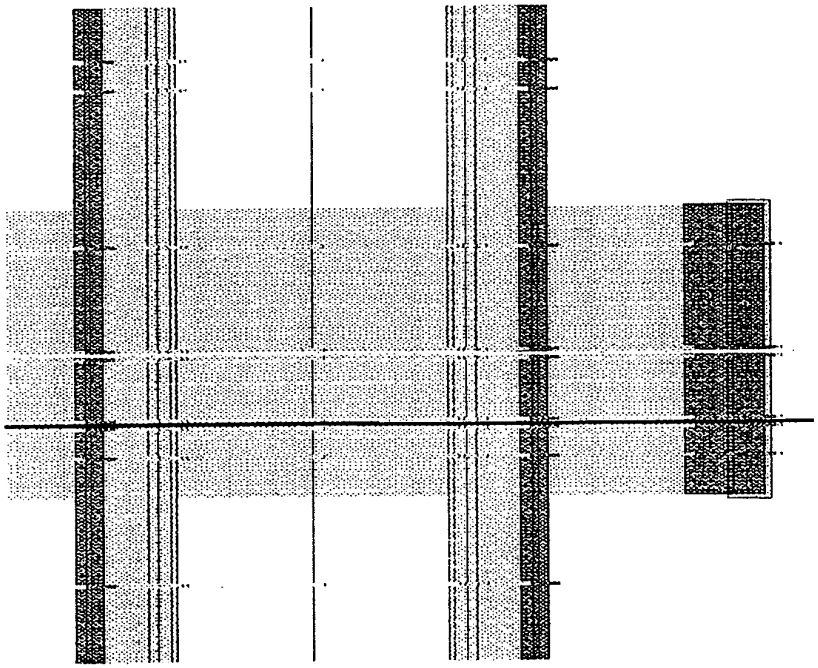

FIG. 5

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/BE 99/00090

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/288 H01L23/48 H01L23/482 H01L23/485

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
4 October 1999	12/10/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	van der Linden, J

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